UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/568,075	02/13/2006	Masaharu Yamamoto	062092	7448

38834 7590 06/09/2009

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
HAN, JONATHAN	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
06/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/568,075	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	JONATHAN HAN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/13/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to the Applicant's communication filed 02/13/2006. In virtue of this communication, claims 1-20 are pending in the instant application.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-3, 5-10, 12-14, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levine (U.S. Patent No. 4,666,796) in view of Kim et al. (U.S. Publication No. 2003/0104651 A1) and Suzuki (Japanese Publication No. 2005-123297 A).

With respect to claim 1, Levine discloses in Figure 2, a hermetic sealing cap [10]

employed for an electronic component storage package including an electronic component storing member for storing an electronic component, comprising: a substrate [12]; a first layer [14], formed on the surface of said substrate, mainly composed of Ni; a second layer formed on the surface of said first layer [18] (Levine Column 3, line 62-Column 4, line 14).

Levine fails to disclose a first layer contains a diffusion accelerator, a solder layer mainly composed of Sn formed on a region of the surface of said second layer to which said electronic component storing member is bonded, wherein said second layer has a function of inhibiting said first layer from diffusing into said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature.

Suzuki discloses a first layer contains a diffusion accelerator (see Paragraph [0033]-[0034]; Cobalt is a diffusion accelerator).

Suzuki fails to disclose a solder layer mainly composed of Sn formed on a region of the surface of said second layer to which said electronic component storing member is bonded, wherein said second layer has a function of inhibiting said first layer from diffusing into said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature.

Kim discloses a solder layer mainly composed of Sn formed on a region of the

surface of said second layer to which said electronic component storing member is bonded (see Paragraph [0031]-[0032])

Kim fails to disclose said second layer has a function of inhibiting said first layer from diffusing into said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature.

While the said second layer has a function of inhibiting said first layer from diffusing into said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature are not explicitly disclosed, it is understood that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

It would have been obvious to one of ordinary skill in the art at the time of invention that the second layer would inherently inhibit the first layer from diffusing into the solder layer at a first temperature as well as diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said storing member at a second temperature higher than said first temperature as both the prior art and the claimed invention are structurally analogous and the structure of the prior art is capable

of performing the intended use. It would have also been obvious to one of ordinary skill in the art at the time of invention to implement a diffusion accelerator in the first layer, of the Levine's cap, as taught by Suzuki in order to control the diffusion of nickel and produce a long term reliability of the layer (see Suzuki, Paragraph [0035]). It would have further been obvious to one of ordinary skill in the art at the time of invention to implement Kim's soldering layer on the system as disclosed by the combination of Levine and Suzuki in order to properly seal and maintain the sealant on the package cap onto the main package compartment (see Kim, Paragraph [0030])

With respect to claim 2, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 1 and further discloses said first temperature is a temperature at a time of forming said solder layer by melting solder paste (see Kim, Paragraph [0032]), and said second temperature is a temperature at a time of bonding said hermetic sealing cap to said electronic component storing member by melting said solder layer (see Kim, Paragraph [0035]).

With respect to claim 3, the combination of Levine, Suzuki, and Kim discloses all material as stated in claims 1 and 2 and further discloses said second layer is made of Ni (see Levine, Column 4, line 9-36).

With respect to claim 5, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 1 and further discloses said first layer contains 7.5 mass% to 20 mass% of Co as said diffusion accelerator (see Suzuki, Paragraph [0033]-[0034]).

With respect to claim 6, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 1 and further discloses said substrate is made of an Fe-Ni-

Co alloy (see Levine, Column 4, lines 46-57).

With respect to claim 7, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 1 and further discloses said first layer and said second layer are formed by plating (see Levine, Column 2, lines 15-23).

With respect to claim 8, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 7 and further discloses said first layer is formed on the whole area of the surface of said substrate, and said second layer is formed on the whole area of the surface of said first layer (see Levine, Figure 2).

With respect to claim 9, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 1 and further discloses said solder layer contains no Pb, and contains Ag (see Kim, Paragraph [0031]).

With respect to claim 10, Levine discloses an electronic component storage package including an electronic component storing member for storing an electronic component, comprising: a hermetic sealing cap [10] including a substrate [12], a first layer [14], formed on the surface of said substrate, mainly composed of Ni, a second layer [18] formed on the surface of said first layer (Levine Column 3, line 62- Column 4, line 14).

Levine fails to teach a first layer containing a diffusion accelerator, a solder layer mainly composed of Sn formed on a region of the surface of said second layer to which said electronic component storing member is bonded, with said second layer having a function of inhibiting said first layer from diffusing into said solder layer at a first temperature while diffusing said first layer into said solder layer through said second

layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature, wherein a third layer is formed on a portion of said electronic component storing member corresponding to said solder layer, said solder layer and said third layer are bonded to each other, and an intermetallic compound containing Sn of said solder layer is formed on the junction between said hermetic sealing cap and said electronic component storing member.

Suzuki teaches a first layer containing a diffusion accelerator (see Paragraph [0033]-[0034]; Cobalt is a diffusion accelerator).

Suzuki fails to teach a solder layer mainly composed of Sn formed on a region of the surface of said second layer to which said electronic component storing member is bonded, with said second layer having a function of inhibiting said first layer from diffusing into said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature, wherein a third layer is formed on a portion of said electronic component storing member corresponding to said solder layer, said solder layer and said third layer are bonded to each other, and an intermetallic compound containing Sn of said solder layer is formed on the junction between said hermetic sealing cap and said electronic component storing member.

Kim teaches a solder layer mainly composed of Sn formed on a region of the surface of said second layer to which said electronic component storing member is bonded (see Paragraph [0031]-[0032]), wherein a third layer [10] is formed on a portion

of said electronic component storing member corresponding to said solder layer, said solder layer and said third layer are bonded to each other, and an intermetallic compound containing Sn of said solder layer is formed on the junction between said hermetic sealing cap and said electronic component storing member (see Figure 5B and Paragraph [0036]-[0037]).

Kim fails to teach with said second layer having a function of inhibiting said first layer from diffusing into said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature

While the said second layer has a function of inhibiting said first layer from diffusing into said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature are not explicitly disclosed, it is understood that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

It would have been obvious to one of ordinary skill in the art at the time of invention that the second layer would inherently inhibit the first layer from diffusing into the solder layer at a first temperature as well as diffusing said first layer into said solder

layer through said second layer when said solder layer bonds to said storing member at a second temperature higher than said first temperature as both the prior art and the claimed invention are structurally analogous and the structure of the prior art is capable of performing the intended use. It would have also been obvious to one of ordinary skill in the art at the time of invention to implement a diffusion accelerator in the first layer, of the Levine's cap, as taught by Suzuki in order to control the diffusion of nickel and produce a long term reliability of the layer (see Suzuki, Paragraph [0035]). It would have further been obvious to one of ordinary skill in the art at the time of invention to implement Kim's soldering layer on the system as disclosed by the combination of Levine and Suzuki in order to properly seal and maintain the sealant on the package cap onto the main package compartment (see Kim, Paragraph [0030])

With respect to claim 12, Levine discloses in Figure 2, a method of manufacturing a hermetic sealing cap employed for an electronic component storage package including an electronic component storing member for storing an electronic component, comprising steps of: preparing a substrate [12]; forming a first layer [14] mainly composed of Ni on the surface of said substrate; forming a second layer [18] on the surface of said first layer (Levine Column 3, line 62- Column 4, line 14).

Levine fails to disclose a first layer containing a diffusion accelerator and forming a second layer on the surface of said first layer; and forming a solder layer mainly composed of Sn on a region of the surface of said second layer to which said electronic component storing member is bonded, wherein the step of forming said second layer includes a step of forming the second layer having a function of inhibiting said first layer

from diffusing into said solder layer when forming said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature.

Suzuki teaches a first layer containing a diffusion accelerator (see Paragraph [0033]-[0034]; Cobalt is a diffusion accelerator)

Suzuki fails to teach forming a solder layer mainly composed of Sn on a region of the surface of said second layer to which said electronic component storing member is bonded, wherein the step of forming said second layer includes a step of forming the second layer having a function of inhibiting said first layer from diffusing into said solder layer when forming said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature.

Kim teaches forming a solder layer mainly composed of Sn on a region of the surface of said second layer to which said electronic component storing member is bonded (see Figure 4, Paragraph [0031]-[0032])

Kim fails to teach wherein the step of forming said second layer includes a step of forming the second layer having a function of inhibiting said first layer from diffusing into said solder layer when forming said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second

temperature higher than said first temperature.

While it is not explicitly disclosed that the second layer having a function of inhibiting said first layer from diffusing into said solder layer when forming said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature, it is understood that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

It would have been obvious to one of ordinary skill in the art at the time of invention that the second layer would function to inhibit said first layer from diffusing into said solder layer when forming said solder layer at a first temperature while diffusing said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature as both the prior art and the claimed invention are structurally analogous and the structure of the prior art is capable of performing the intended use. It would have also been obvious to one of ordinary skill in the art at the time of invention to implement a diffusion accelerator in the first layer, of the Levine's cap, as taught by Suzuki in order to control the diffusion of nickel and produce a long term reliability of the layer (see Suzuki, Paragraph [0035]). It would have further been obvious to one of ordinary skill in the art at the time of invention to implement Kim's

formation of a soldering layer on the system as disclosed by the combination of Levine and Suzuki in order to properly seal and maintain the sealant on the package cap onto the main package compartment (see Kim, Paragraph [0030])

With respect to claim 13, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 12 and further discloses the step of forming said solder layer includes steps of arranging solder paste mainly composed of Sn on a region of the surface of said second layer to which said electronic component storing member is bonded and forming said solder layer mainly composed of said Sn by melting said solder paste at said first temperature (see Kim Figure 4, and Paragraph [0030]).

With respect to claim 14, the combination of Levine, Suzuki, and Kim discloses all material as stated in claims 12 and 13 and further discloses, wherein said second layer is made of Ni (see Levine, Column 4, line 9-36).

With respect to claim 16, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 12 and further discloses said first layer contains 7.5 mass % to 20 mass % of Co as said diffusion accelerator (see Suzuki, Paragraph [0033]-[0034]).

With respect to claim 17, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 12 and further discloses, said substrate is made of an Fe-Ni-Co alloy (see Levine, Column 4, lines 46-57).

With respect to claim 18, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 12 and further discloses the step of forming said first layer includes a step of forming said first layer by plating, and the step of forming said second

layer includes a step of forming said second layer by plating (see Levine, Column 2, lines 15-23).

With respect to claim 19, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 18 and further discloses the step of forming said first layer by plating includes a step of forming said first layer on the whole area of the surface of said substrate, and the step of forming said second layer by plating includes a step of forming said second layer on the whole area of the surface of said first layer (see Levine, Figure 2).

With respect to claim 20, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 12 and further discloses wherein said solder layer contains no Pb, and contains Ag (see Kim, Paragraph [0031]).

4. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levine (U.S. Patent No. 4,666,796) in view of Kim et al. (U.S. Publication No. 2003/0104651 A1) and Suzuki (Japanese Publication No. 2005-123297 as applied to claims 1-3 and 12-14 above, and further in view of Woolhouse et al. (U.S. Patent No. 4,236,296; hereinafter referred to as Woolhouse).

With respect to claim 4, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 3 but fails to disclose said second layer has a thickness of at least 0.03 μm and not more than 0.075 μm.

Woolhouse discloses said second layer has a thickness of at least 0.03 μm and not more than 0.075 μm (see Column 3, lines 14-18; thin plating using nickel).

It would have been obvious to one of ordinary skill in the art at the time of

invention to implement a second layer within the range of at least 0.03 μm and not more than 0.075 μm in order to produce a layer that is both thick enough to properly passivate the layers below while thin enough for allowing for proper placement of the layer (see Column 3, lines 36-43)

With respect to claim 15, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 14 but fails to disclose said second layer has a thickness of at least 0.03 μm and not more than 0.075 μm

Woolhouse discloses said second layer has a thickness of at least 0.03 μm and not more than 0.075 μm (see Column 3, lines 14-18; thin plating using nickel).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement a second layer within the range of at least 0.03 μm and not more than 0.075 μm in order to produce a layer that is both thick enough to properly passivate the layers below while thin enough for allowing for proper placement of the layer (see Column 3, lines 36-43)

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levine (U.S. Patent No. 4,666,796) in view of Kim et al. (U.S. Publication No. 2003/0104651 A1) and Suzuki (Japanese Publication No. 2005-123297 A) as applied to claim 10 above, and further in view of Shiomi et al (U.S. Publication No. 2004/0023487 A1; hereinafter referred to as Shiomi).

With respect to claim 11, the combination of Levine, Suzuki, and Kim discloses all material as stated in claim 10 and further discloses a portion of said second layer corresponding to the junction between said hermetic sealing cap and said electronic

component storing member diffuses in said intermetallic compound, but fails to disclose the junction between said hermetic sealing cap and said electronic component storing member contains an intermetallic compound consisting of an Ni-Sn alloy.

Shiomi teaches the junction between said hermetic sealing cap and said electronic component storing member contains an intermetallic compound consisting of an Ni-Sn alloy (see Paragraph [0013]).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shiomi's junction containing an Ni-Sn alloy in order to quickly form a compound at a low temperature and suppress deterioration in the characteristics of the electronic component due to heating performed for the fusion welding. (see Shiomi Paragraph [0013]).

Citation of Pertinent Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Matsubara et al (U.S. Publication No. 2005/0023661 A1) discloses a hermetically sealing cap with multiple plating layers.

Hirose et al (U.S. Patent No. 5,898,218) discloses a ceramic package with a hermetically sealed cap.

Slattery (U.S. Patent No. 4,737,418) discloses a lid for closing semiconductor packages using nickel.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONATHAN HAN whose telephone number is (571)270-7546. The examiner can normally be reached on Monday through Friday 8:30 AM - 6 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571)272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JONATHAN HAN/
Examiner, Art Unit 2818
05/29/2009

/Steven Loke/

Supervisory Patent Examiner, Art Unit 2818